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A TWO-CHANNEL ANALOG-TO-DIGITAL CONVERTER FOR THE TEKTRONIX 909 SCIENTIFIC CALCULATOR

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Monterey, California

THESIS

A Two-Channel Analog-to-Digital Converter
for
The Tektronix 909 Scientific Calculator

by

Harold C. Schleicher

Thesis Advisor: R. Panholzer

December 1972

A Two-Channel Analog-to-Digital Converter

For the Tektronix 909 Scientific Calculator

by

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December 1972

ABSTRACT

The design and construction of an analog-to-digital converter for interface with the Tektronix 909 Scientific Calculator was undertaken. Use of the calculator was greately enhanced in the area of data processing by allowing on-line sampling and processing of two simultaneous signals.

An investigation into the feasibility of using the 909, the A/D, and a D/A in the simulation of sampled data systems, or as a digital controller for a continuous plant was conducted.

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I. INTRODUCTION

This thesis reports on a two-part project. The first part was the design and construction of an analog-to-digital converter (A/D) for the Tektronix 909 Scientific Calculator. The second part was the testing of an assembly comprised of the A/D, the 909 calculator, and a digital-to-analog converter (D/A). The purpose of the test was to investigate the feasibility of using the 909 and the converters in a hybrid computer configuration to simulate a sampled data control system, or as a digital controller for a continuous plant.

II. THE ANALOG-TO-DIGITAL CONVERTER

A. A/D CONVERTERS

There are several ways of classifying A/D converters. Characteristics typically evaluated include accuracy, complexity, and cost. The major categories of A/D converters and their prime attributes are listed in Table I below. Since A/D conversion has been the topic of many tests, an indepth presentation is not given here; however, Refs. 1-3 are cited for detailed design techniques.

Category	Attribute
Programed	Fixed conversion time
Non-programed	Fast
Open-loop	Fast
Feedback	Few components
Linear ramp	Simple design
Discrete level	Accurate

TABLE I A/D CONVERTERS AND ATTRIBUTES

B. ACCURACY, APERTURE, AND FREQUENCY

Aperture is the period during which the measured signal is being sampled. If sample-hold circuits are employed ahead of the A/D, the aperture can be extremely short. If no sample-hold circuit is used, the aperture is the same as the conversion time of the converter.

Accuracy is related inversley to aperture, i.e., the wider the aperture, the more the measured signal can change during the sample time. Change (slew rate) in the measured signal is related to it's highest frequency component. Equation II-1 gives maximum error as a function of aperture, converter range, and frequency.

$$\text{MAX ERROR} = A \times R \times 2 \times F \qquad \text{II-1}$$

where A = Aperture in seconds

R = Peak-to-peak range of the converter in volts

F = Highest Frequency content in Hz.

C. THE ANALOG-TO-DIGITAL CONVERTER FOR THE TEKTRONIX 909

The dual-channel A/D which was designed for the 909 is classified as a programed, feedback, discrete-level converter. The "fast" integrated circuits used in the converter yield a conversion time of 5.0 microseconds for each channel. The channels are alternately addressed by an analog multiplexer. The attributes of this converter are, accuracy, speed and few components (inexpensive).

1. The A/D uses the method of suecessive approximation. A voltage is generated internally which is one half of the input range for the initial comparison, and half of the previous voltage for each subsequent comparison. For this A/D the initial voltage represents the value 10.22. It is added to the lower limit of the A/D which is -10.22. This means that the first comparison in the A/D conversion cycle determines whether the signal being measured is positive or negative. After ten successive comparisons have been made, the

signal being measured has been bracketed to within .02 volts. Ten binary bits represent the signal. The first binary bit is the sign and the remaining nine bits are the magnitude of the signal or the one's complement of the magnitude depending on the sign. The conversion technique and the sign dependence of the data can be best understood through an example. If the signal is positive the first bit will be held high after the first comparison is complete. The voltage 10.22 will remain added to the -10.22 base voltage. For the second comparison a voltage of 5.11 volts, if the measured signal is greater than 5.11 volts, this voltage will also be kept and the second binary bit will be held high. If the measured signal is between 0.00 and 5.11 volts, the 5.11 volts will not be kept and second binary bit will be set low. Subsequent comparisons are done in a similar manner. If the sign is positive, then the second bit being high means the value is between 5.11 and 10.22 volts, but if the sign is a negative, then the second bit being high means the value is between 0.0 and -5.11 volts. Therefore, whenever a negative voltage is converted, the one's complement of the magnitude bits must be taken. This sign dependence is taken care of in the processor section of the interface.

2. Specifications

The specifications for the A/D converter are listed in Table II. The output of the converter is represented by 10 binary bits. Including the sign, there are $2^{10} = 1024$ distinct levels. The input signal limits are +10.22 to -10.22 giving a range of 20.44 volts.

Dividing this range by the number of levels gives an accuracy of .02 volts. Applying this accuracy figure to Equation II-1 and solving for maximum frequency gives a value greater than 30 Hz. A question arises concerning the fact that there are 1024 levels and yet the range of the converter is $\pm$10.22 volts. This occurs because the converter rounds down and the meaning of the value 10.22 is that the signal is between 10.22 and 10.24 volts. Similarly, a value of 0.0 indicates that the signal is between $\pm$.02 volts.

RANGE	$\pm$10.22 volts
ACCURACY	$\pm$.02 volts
FREQUENCY (maximum)	30 Hz
SLEW RATE (maximum)	188 volts-per-second

TABLE II Specifications for the Analog-to-digital Converter

3. Signal Flow

Figure 1. is a block diagram of the analog-to-digital converter. The control section of the A/D contains a clock which generates clock pulses at a rate of 2 MHZ. A single pulse termed BIT-1 and having a width of one clock cycle is generated each eleventh clock pulse. Strobe pulses (STB) are generated midway between each clock cycle, i.e. with the negative going edge of the clock pulse.

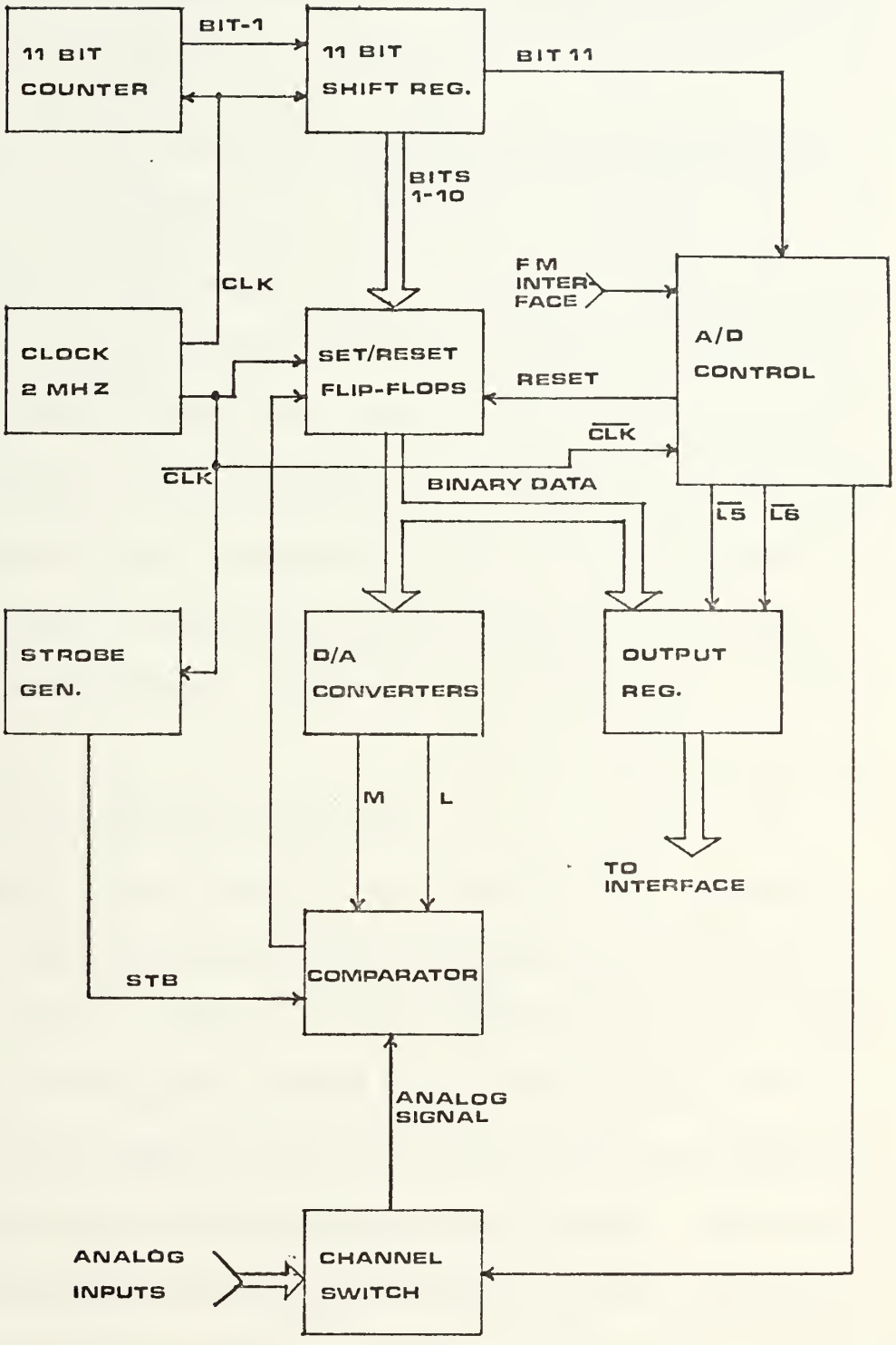
The BIT-1 pulse is shifted from left to right through the eleven-bit shift register by clock pulses. As the BIT-1 pulse passes through

the register it sets the set/reset flip-flop associated with that position. Each flip-flop in turn gates an associated bit in one of the D/A's. A current is generated by the D/A with magnitude proportional to the bit it represents. This current is compared with the input analog signal in the comparator.

The strobe pulse (STB) interrogates the comparator to determine if the newly generated current exceeds the input analog signal. If it does, a clear pulse (CLR) is sent to the associated flip-flop to reset it thereby suppressing the current. If the generated current does not exceed the input analog signal, no CLR pulse is sent, the flip-flop remains set, and the current continues to flow.

When the BIT-1 pulse reaches the eleventh position in the shift register, the A/D conversion is complete. A signal from the A/D controller latches the binary data into the appropriate output register and connects the second input signal to the A/D..

The output data is in the form of binary bits which represent the states of the set/reset flip-flops at the end of the conversion cycle. The remaining nine bits indicate the magnitude of the signal. Detailed circuit diagrams are contained in Appendix A.



NOTE : BROAD ARROWS INDICATE MULTIPLE LINES

FIG.1 A/D BLOCK DIAGRAM

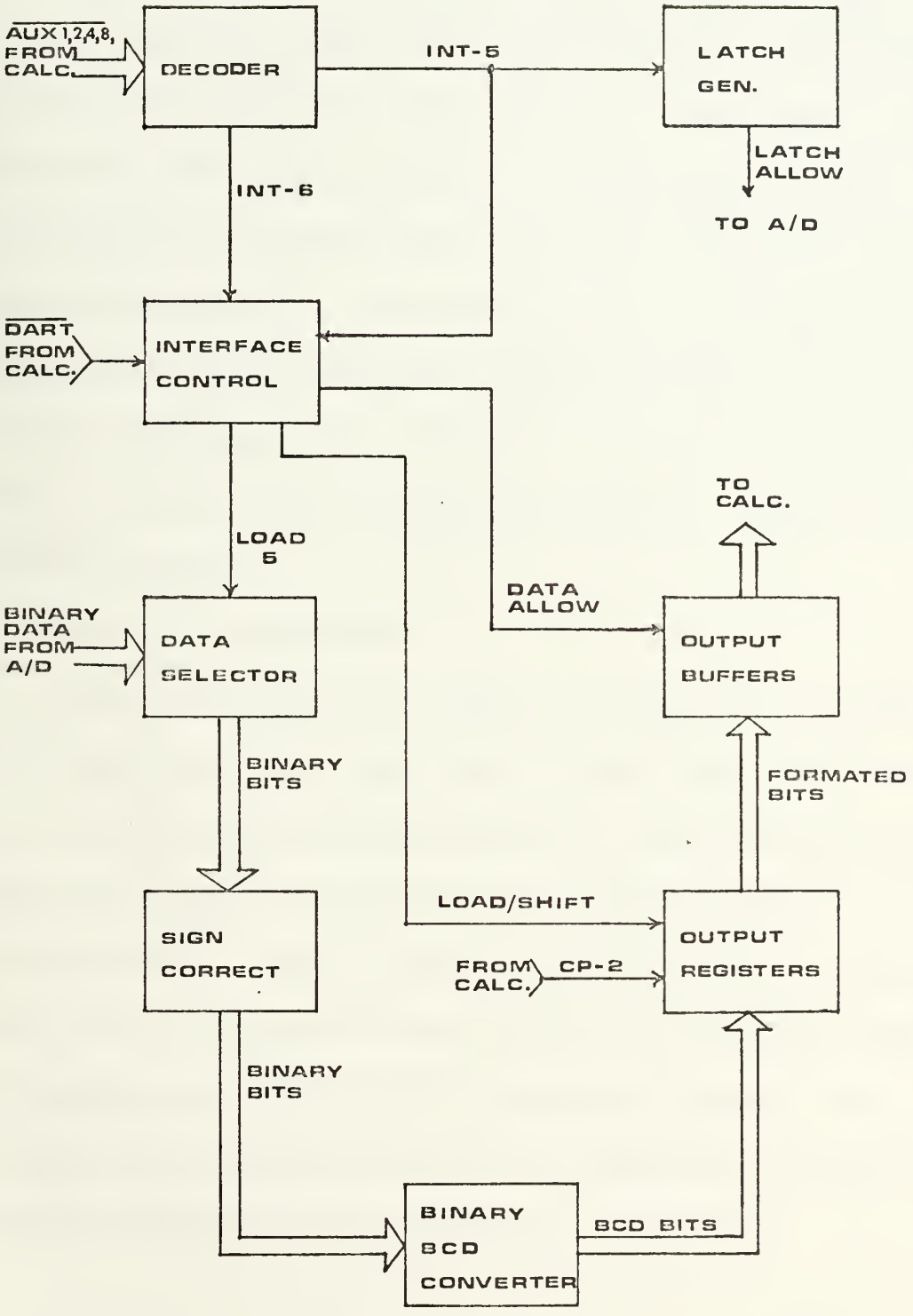
III. INTERFACE OF THE A/D WITH THE 909 CALCULATOR

A. SIGNAL FLOW AT THE INTERFACE

Figure 2 is a block diagram of the interface which consists of two sections: a control section, and a processing section. The controlling section decodes signals from the calculator, latched the binary data into the output registers of the A/D, and sends a "data-select" signal to the final buffers in the data processing section when the calculator indicates that data should be sent. The data processor section selects the data for the appropriate channel, modifies the magnitude bits depending on the sign bit, converts the binary data to binary-coded-decimal (BCD) data, and places it in proper format for input to the calculator.

B. INTERFACE CONTROL SECTION

Signals from the calculator which indicate that a peripheral device has been directly addressed are presented on the $\overline{\text{AUX-1, 2, 4, 8}}$ and AUX-R lines. The decoder, by means of combinational circuitry, determines whether either channel five or channel six has been interrogated. The addresses R_5 and R_6 can be set to other single digits by appropriate cross connections on the address header. A pulse which has the same duration as the interrogating AUX pulses is generated and is termed INT-5 or INT-6 accordingly. Channel five is considered the master channel. Whenever it is interrogated, a "latch allow"



NOTE: BROAD ARROWS INDICATE MULTIPLE LINES

FIG.2 INTERFACE BLOCK DIAGRAM

pulse is generated and the binary data for both channels is latched into the output registers of the A/D. Another pulse which is triggered by the interrogation of channel five is the "load-5"pulse. This pulse is sent to the data selectors in the processor and allows channel five's binary data to flow into the processor. The occurence of either INT-5 or INT-6 generates a pulse (INT) which indicates that data is to be passed to the calculator. This pulse is AND'ed with a signal from the calculator. (DART) and generates a signal (DATA ALLOW) which passes the data at the proper time. This DATA ALLOW pulse is necessary in order to make the converter compatible with other peripherals that are available for the 909.

C. INTERFACE PROCESSOR

The processor uses "data selectors" to make the data selection and the sign correction. Read-only-memories (ROM's) are used to convert the nine binary bits into BCD form. The output of the ROM's is fed into the required locations in four eight-bit shift registers so that when the DART signal is received from the calculator, the data will be transferred from the shift registers through the final buffers to the input data lines $\overline{\text{DIN-1, 2, 4, 8}}$ of the 909. Detailed diagrams of the circuitry of the interface are presented in Appendix B. Reference 4 contains additional signal flow information for the 909.

IV. PROGRAMMING THE 909 FOR A/D CONVERSION

A. DIRECT ADDRESSING WITH THE 909

Addressing a peripheral device with the 909 can be accomplished either directly or indirectly. The indirect method is a relatively slow process and is not used in conjunction with this A/D unit. Further information on indirect addressing is available in Reference 4. Direct addressing, which can be accomplished in the fast mode of the calculator, makes use of the "REMOTE" button. For example, in order to address A/D channel 5, one simply presses keys REMOTE 5 , normally written R_5. This action simultaneously locks data for channels 5 and 6 into the output registers of the A/D and feeds the value for channel five into the calculator. To get the value for channel six, one presses R_6. The data for each channel is measured alternately by the A/D. The latch which locks both values into appropriate output buffers is activated by a 12-micro-second pulse. New values (data update) are obtained only when channel five is interrogated. Interrogating channel six will continue to repeat the same value for channel six.

B. CONVERSION CONSTANT

Preamplifiers have been installed at the inputs of the A/D for both channels. Their purpose is to allow adjustment of individual channel gains and balances. The gain in these preamps affects the analog signal before it gets to the converter therefore, a conversion

constant is used in the calculator to make the data bits represent the analog signal. In order to simplify programming, the gains are adjusted so that a 10.22-volt analog input is represented by 5.11 in data bits. The conversion constant is 2.0. By changing the gain of the preamps one can realize a variety of ranges and accuracies for the converter. (See paragraph II.2 for the relationship of the error to amplitude and signal frequency content.)

C. A TYPICAL PROGRAM FOR THE 909

A typical program for the 909 calculator is given below. Each box or character represents the depressing of a key. The underlined step, although not necessary, is included for clarity.

DEF f (x)

$R_5 \times K_{21} = K_{23}$

$R_6 \times K_{22} = K_{24}$

$K_{24} + K_{23} = R_1 = R_2$ DEF f (x)

R_5 and R_6 address the A/D and cause the appropriate values to be presented to the calculator. K_{21} and K_{22} are constants stored in the calculator prior to implementing the program. They contain the conversion factor of 2.0 and any other multiplication factor which may be desired. K_{23} and K_{24} are storage locations for the results of the intermediate multiplications. R_1 and R_2 are the addresses for the X and Y outputs respectively of the D/A and are used in conjunction with an X-Y plotter. If the D/A is not to be used, the last line in the three given above is $K_{24} + K_{23} = K_{25}$ DEF f (x). The final value will then be presented in the calculator display.

V. TESTING PROCEDURES AND RESULTS

Figure 3 is a block diagram of the test assembly used to investigate the feasibility of using the A/D, the 909, and a D/A in a hybrid computer configuration for simulation of sampled data systems or as a digital controller for a continuous plant.

A. FREQUENCY RESPONSE

Sinusoidal signals of different frequencies and amplitudes were fed into the test system. A modification of the program given in paragraph IV. C. was used; the last line being $K_{23} + 3 = R_1$ DEF f (x). The results of this test indicated that for a given frequency, the output from the D/A deteriorates as amplitude is increased. Similarly, for a given amplitude, the output deteriorates as the frequency is increased. The deterioration is due to a mechanism in the D/A which locks the system into an "idle" condition while the D/A conversion is performed. The D/A conversion technique is such that the conversion time is a function of change in the output signal. Figure 4 shows the deterioration that occurs for a 4 volt peak-to-peak sinusoid as the frequency is increased.

B. SYSTEM DELAY

To demonstrate system delay, a sawtooth waveform of 4 volts peak-to-peak was used. The input analog signal was applied to the X input of an X-Y plotter. The processed signal was fed to the Y input.

As indicated in paragraph V. A. above, the conversion time of the D/A is a function of signal slew rate. Figure 5 shows the increased delay due to an increase in slew rate as well as the deterioration which occurs.

C. SUMMARY

The analog-to-digital converter and the Tektronix 909 Scientific Calculator constitute an extremely powerful on-line data processor. The limitations of this data processor are those specified in Table II.

The A/D, 909, and D/A connot be used in conjunction with sampled data systems either simulated or actual. The prime factor which impedes such use is the D/A because of the interplay of output signal slew rate, delay, and sample rate.

With the advent of new modular "fast" D/A's, it is recommended that a modular D/A as shown in Figure 6 be assembled and interfaced with the Calculator. The D/A and interface shown use the same addressing technique as the A/D. It is for use with direct addressing and does not hold the calculator while conversion is taking place.

D. ACKNOWLEDGEMENTS

The support of Tektronix, Inc., especially that of Mr. Jack Grimes, was paramount in the realization of the working analog-to-digital converter. In addition, the support of Signetics Corporation, Especially Mr. R. Trout and Mr. G. Schlit, were greatly appreciated.

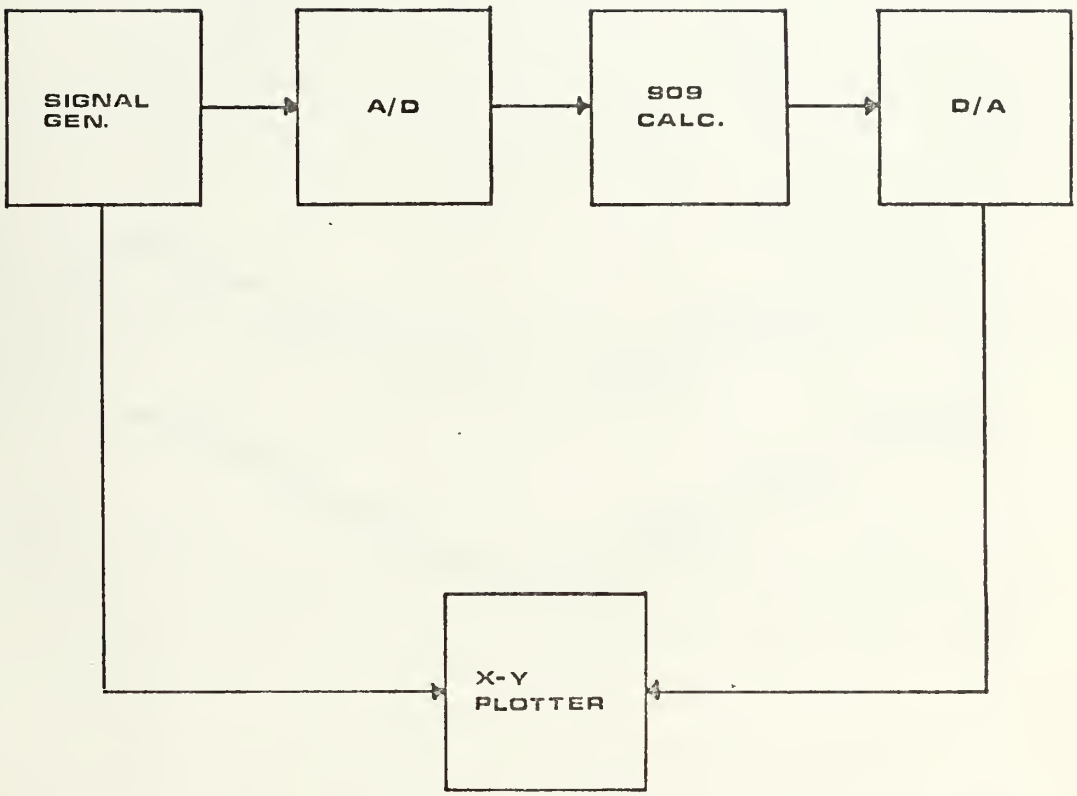


FIG.3 TEST ASSEMBLY BLOCK DIAGRAM

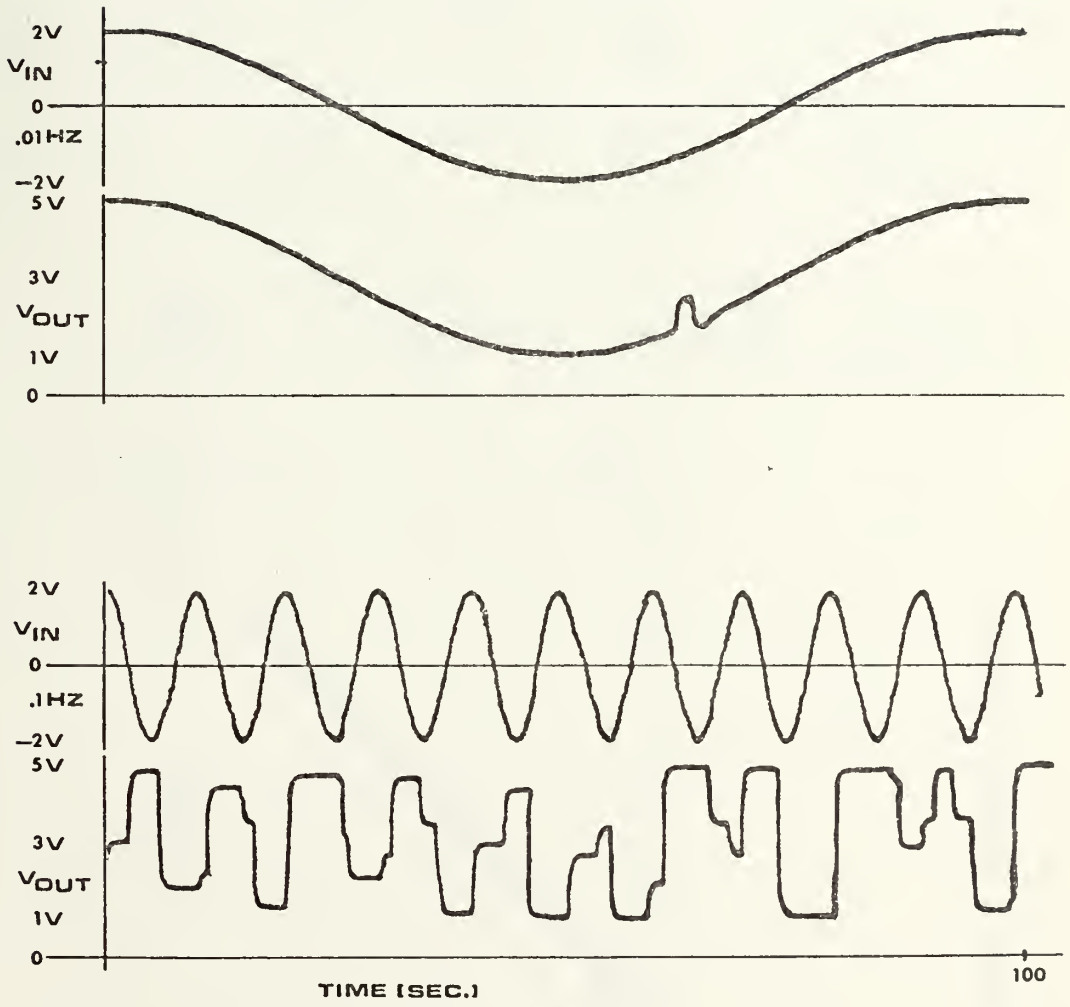


FIG.4 INPUT AND OUTPUT PLOTS

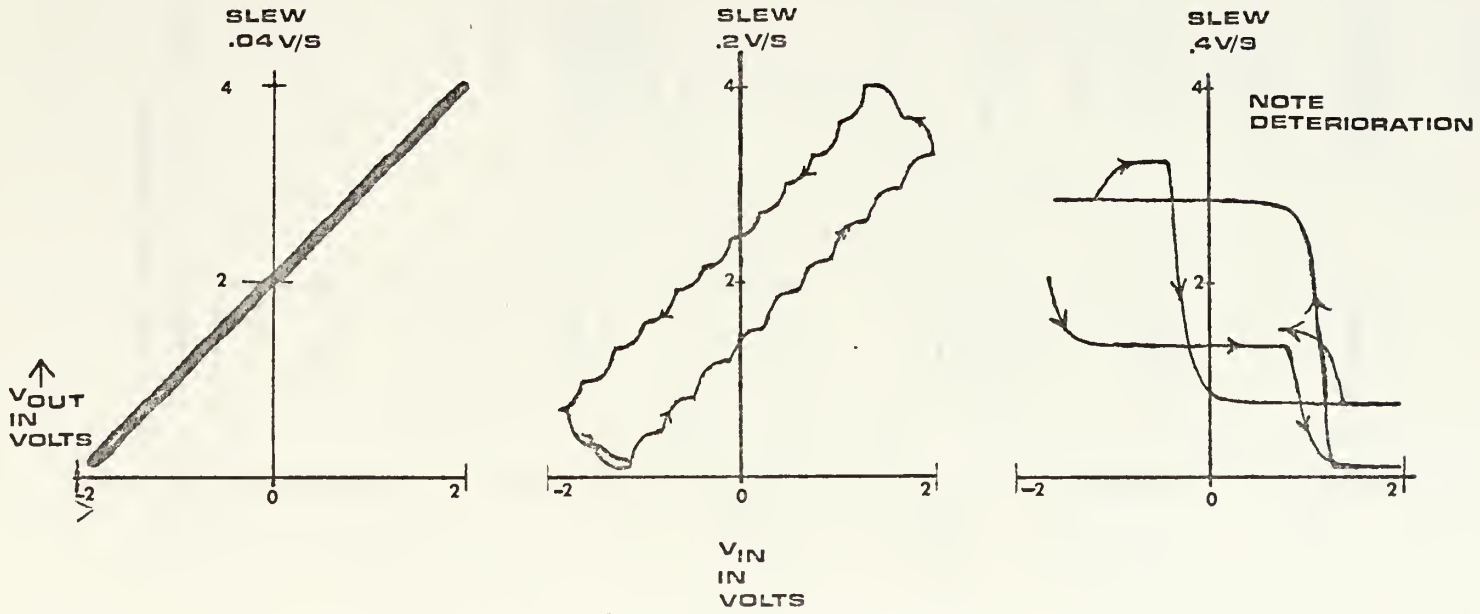
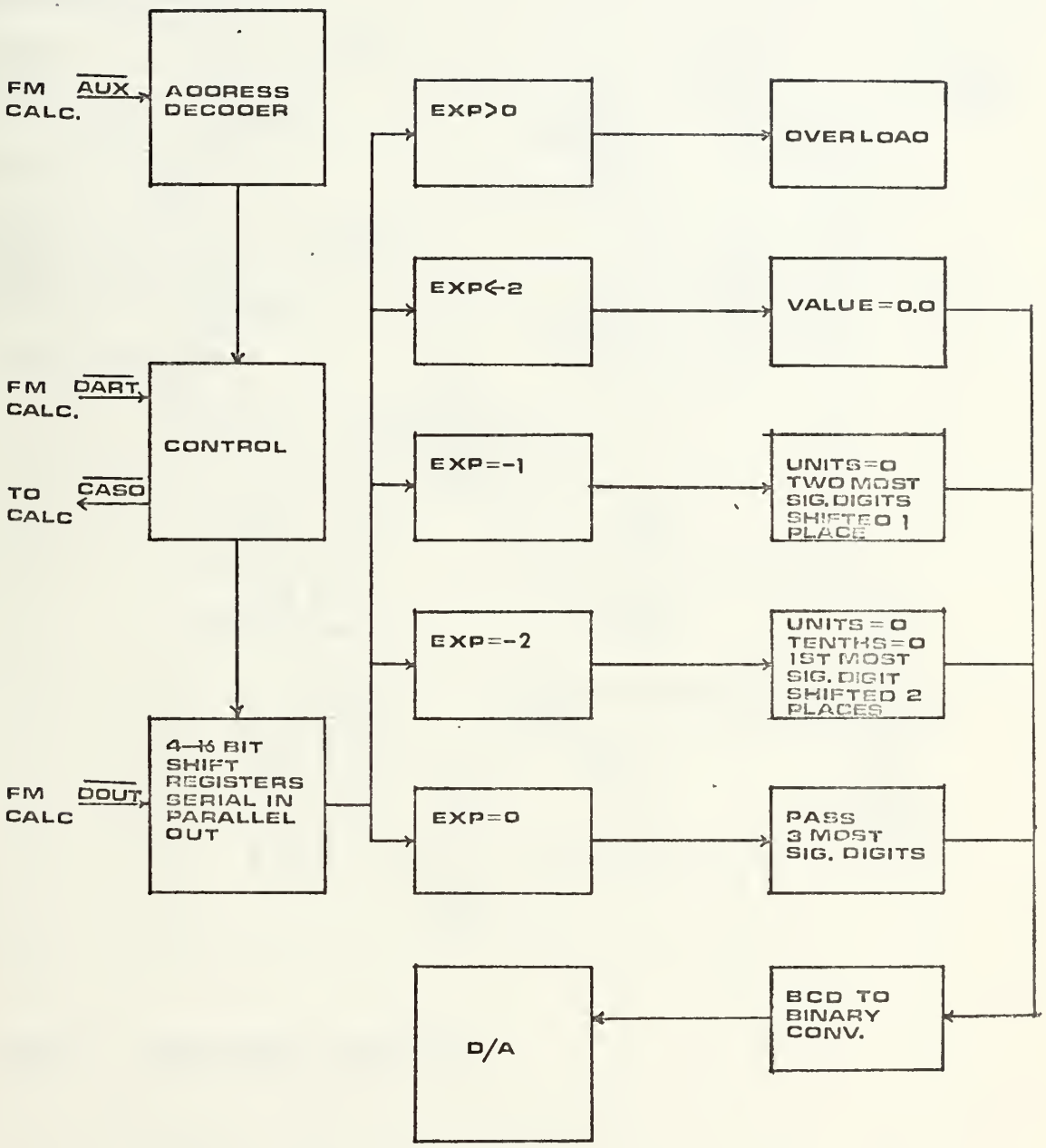


FIG.5 DELAY PLOTS



NOTE: DATA IN SCIENTIFIC NOTATION
RANGE ±9.99 VOLTS

FIG.6 BLOCK DIAGRAM OF PROPOSED D/A

APPENDIX A

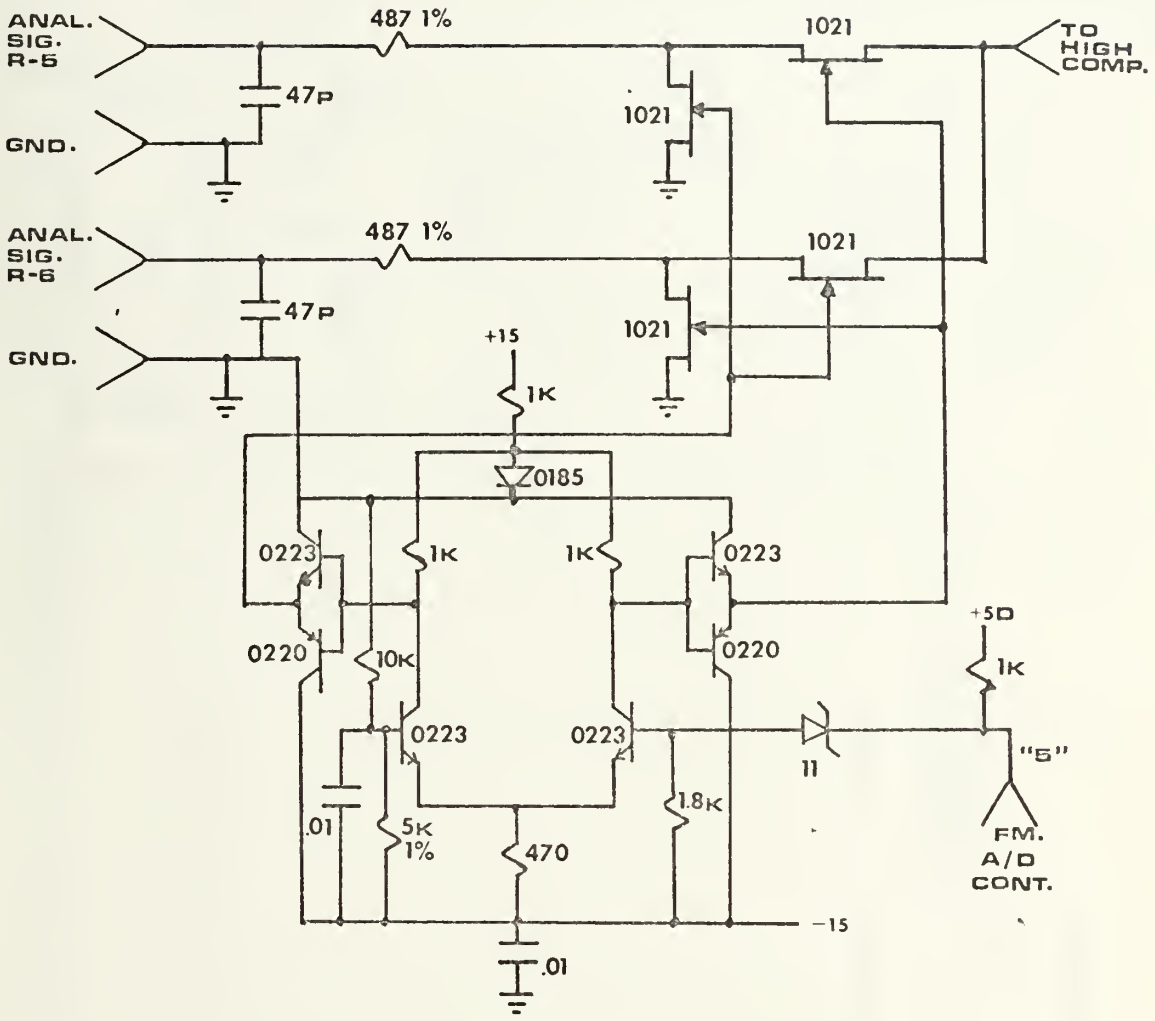


FIG.7 CHANNEL SWITCH

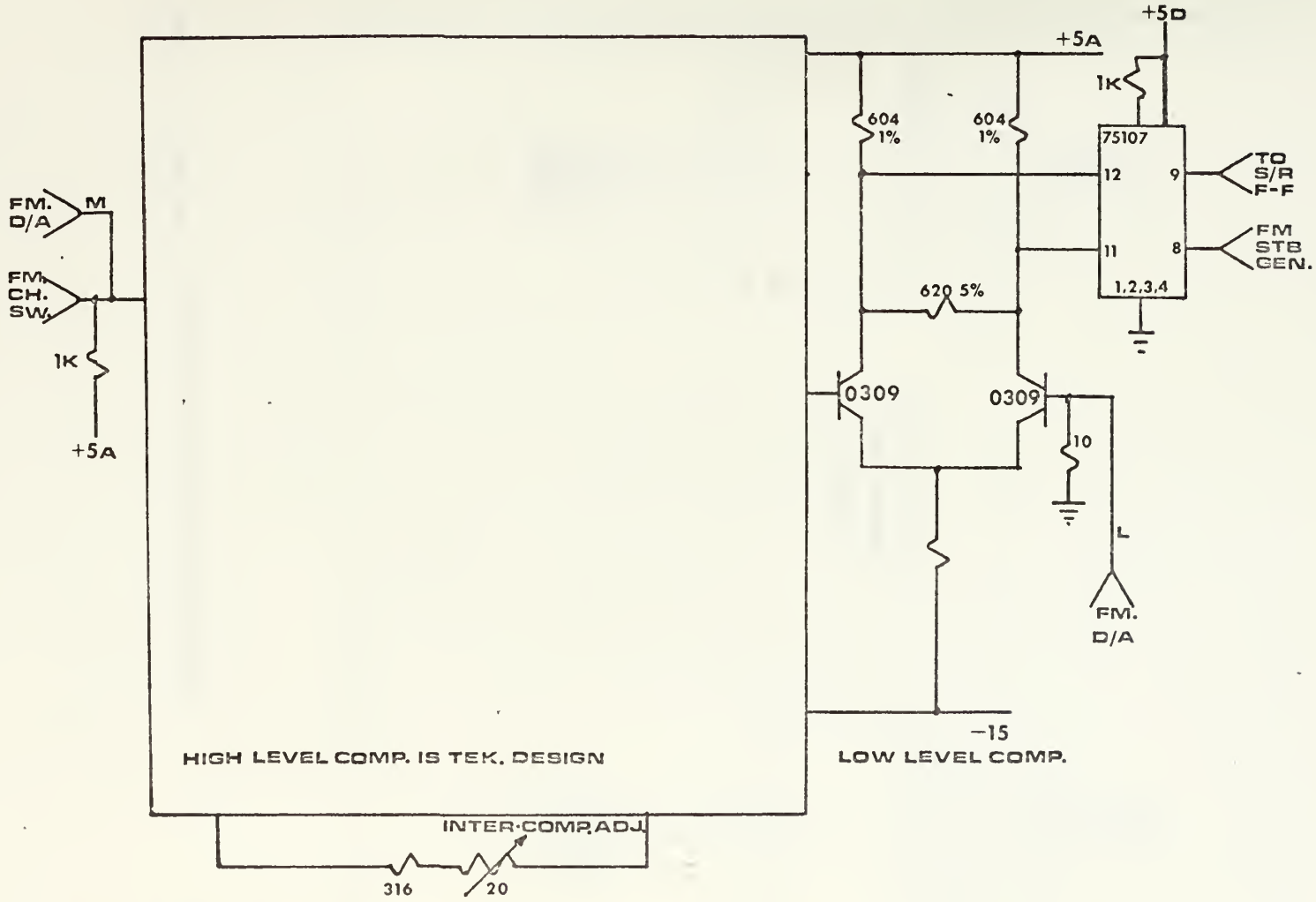


FIG. 8 COMPARATORS

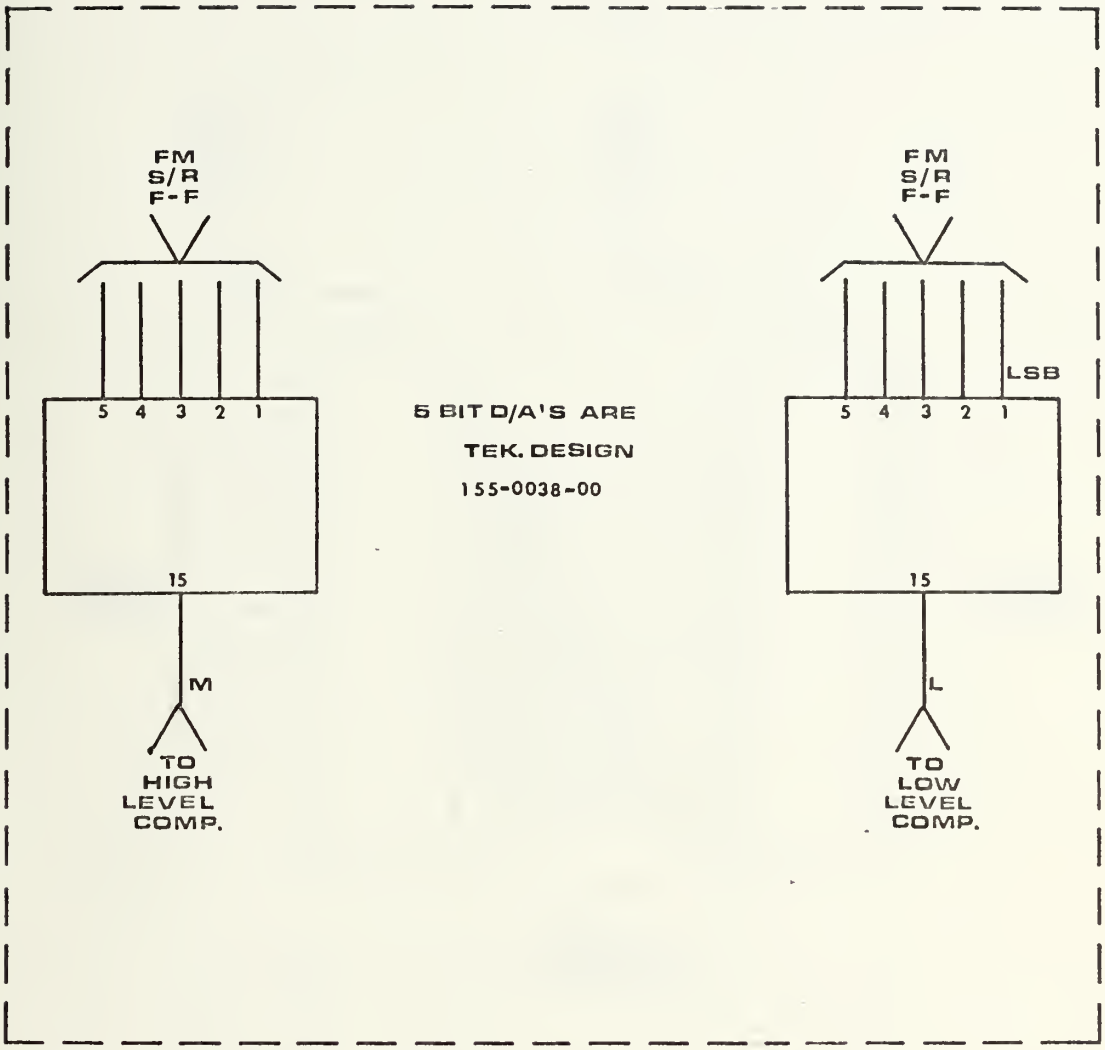


FIG.9 DIGITAL TO ANALOG CONVERTERS

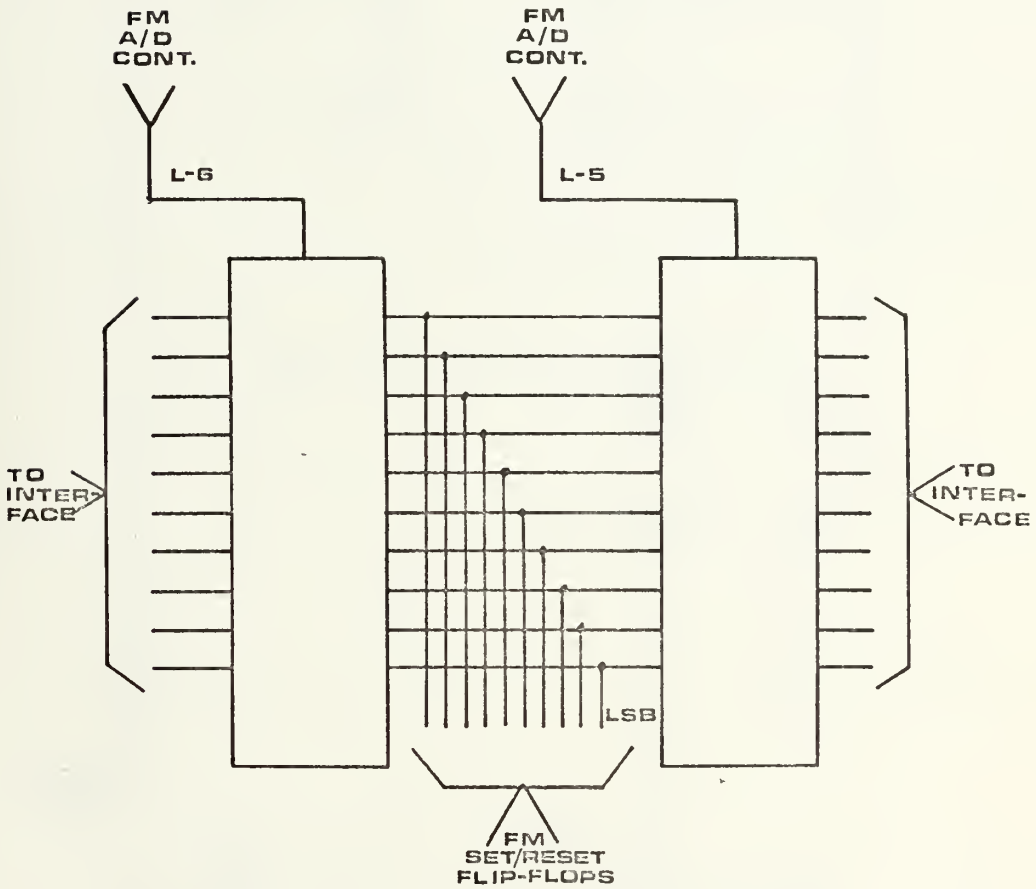


FIG.10 OUTPUT REGISTERS

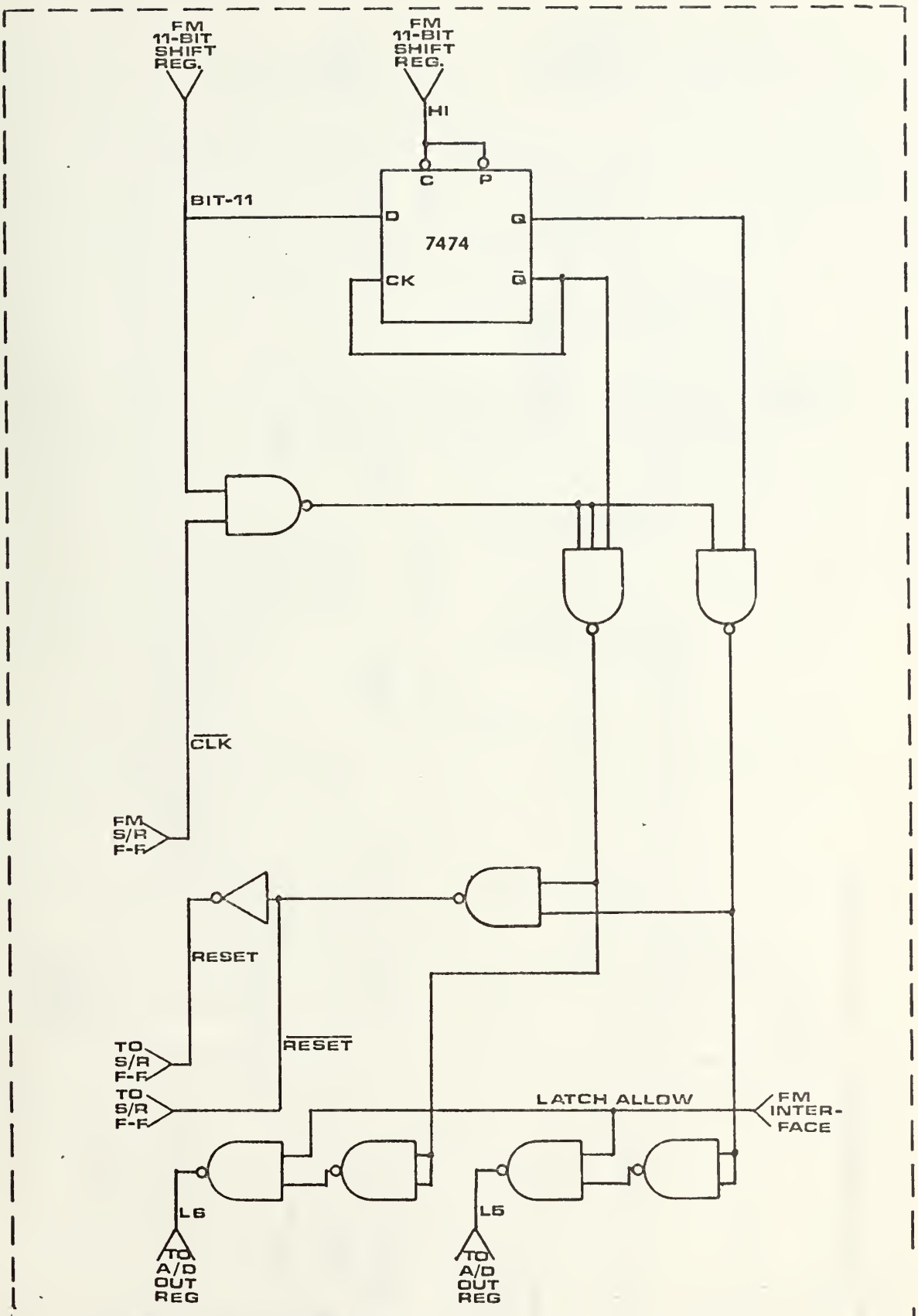


FIG.11 A/D CONTROL

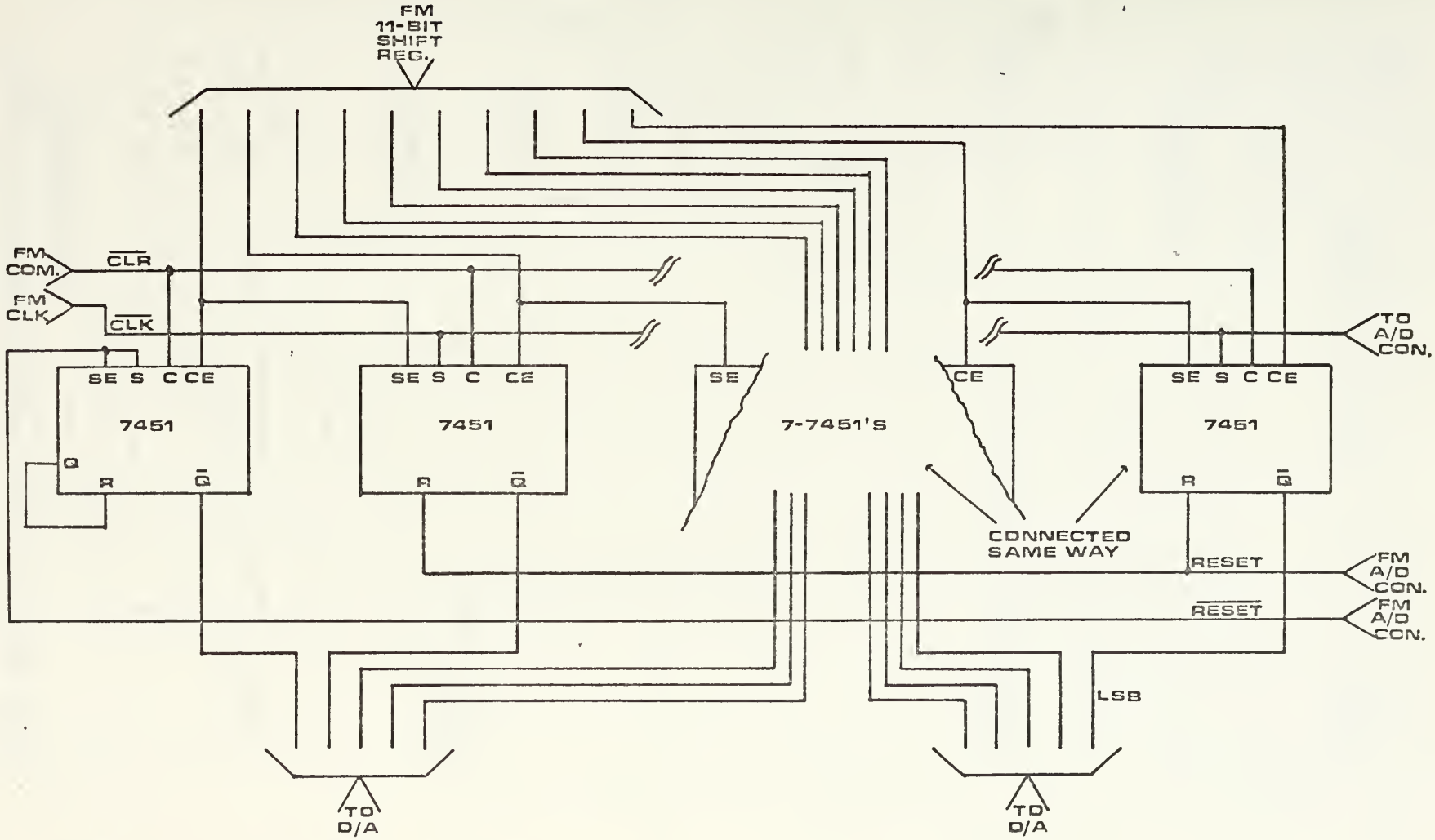


FIG.12 SET/RESET FLIP-FLOPS

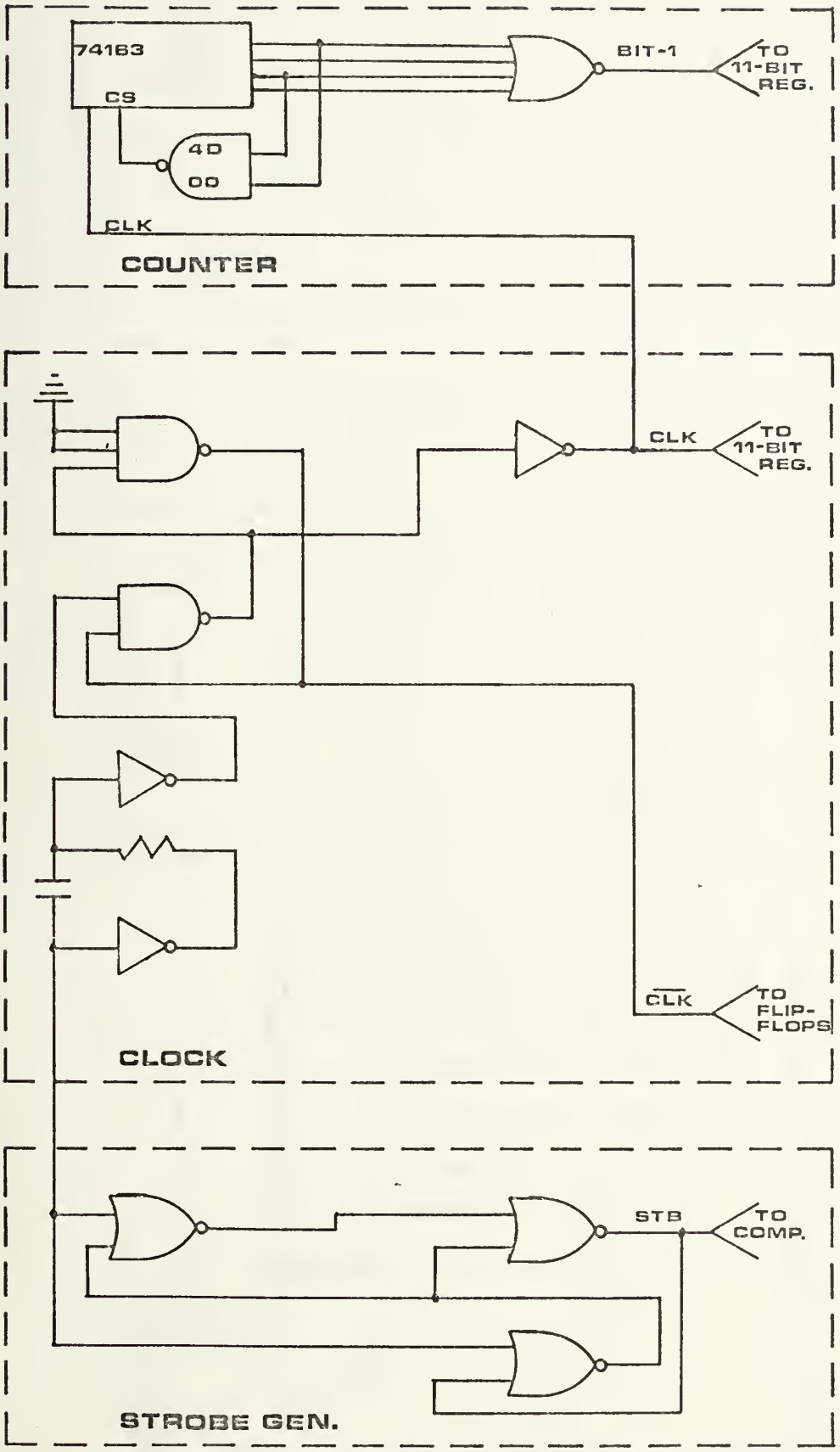


FIG.13 COUNTER, CLOCK, AND STROBE GEN.

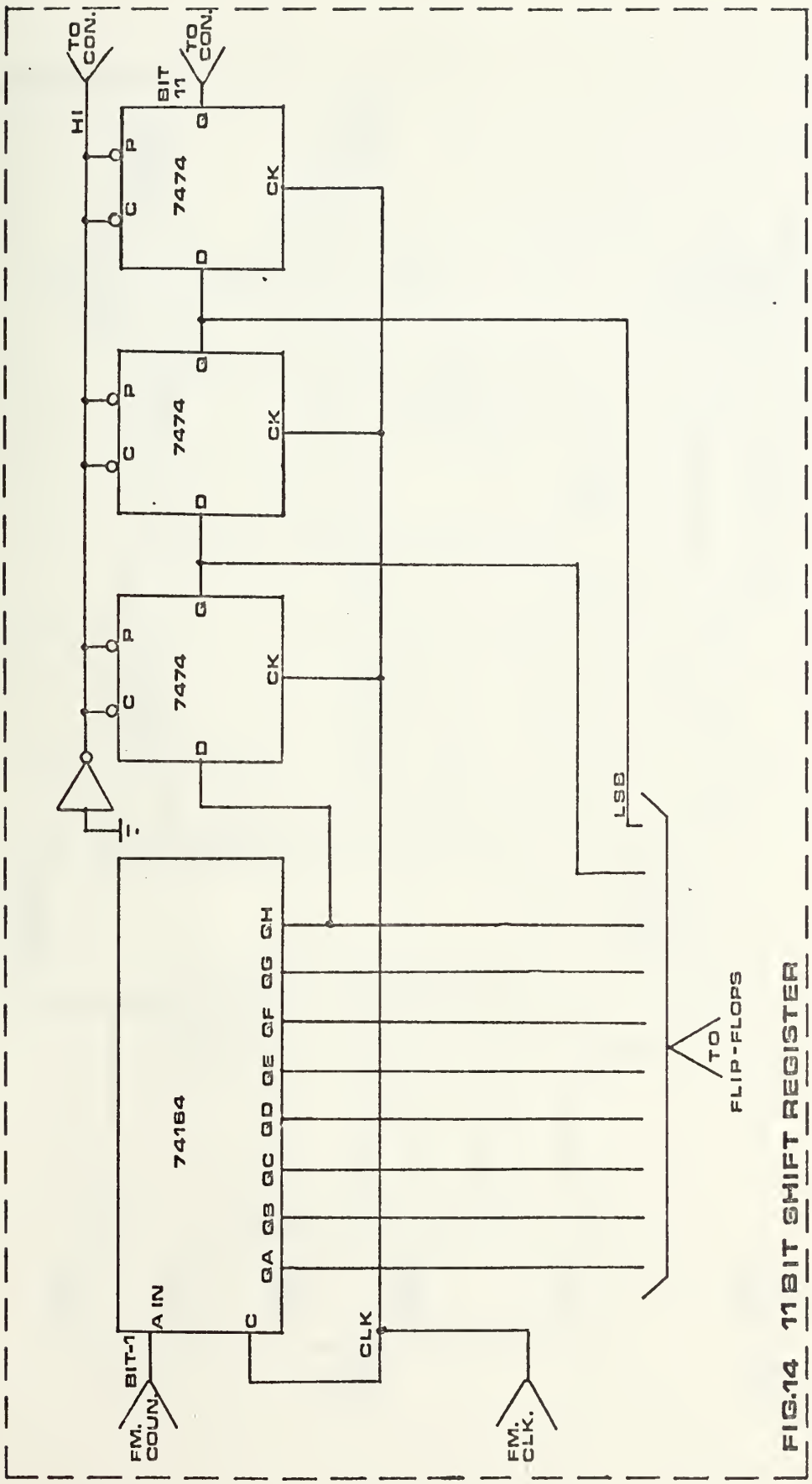


FIG.14 11 BIT SHIFT REGISTER

APPENDIX B

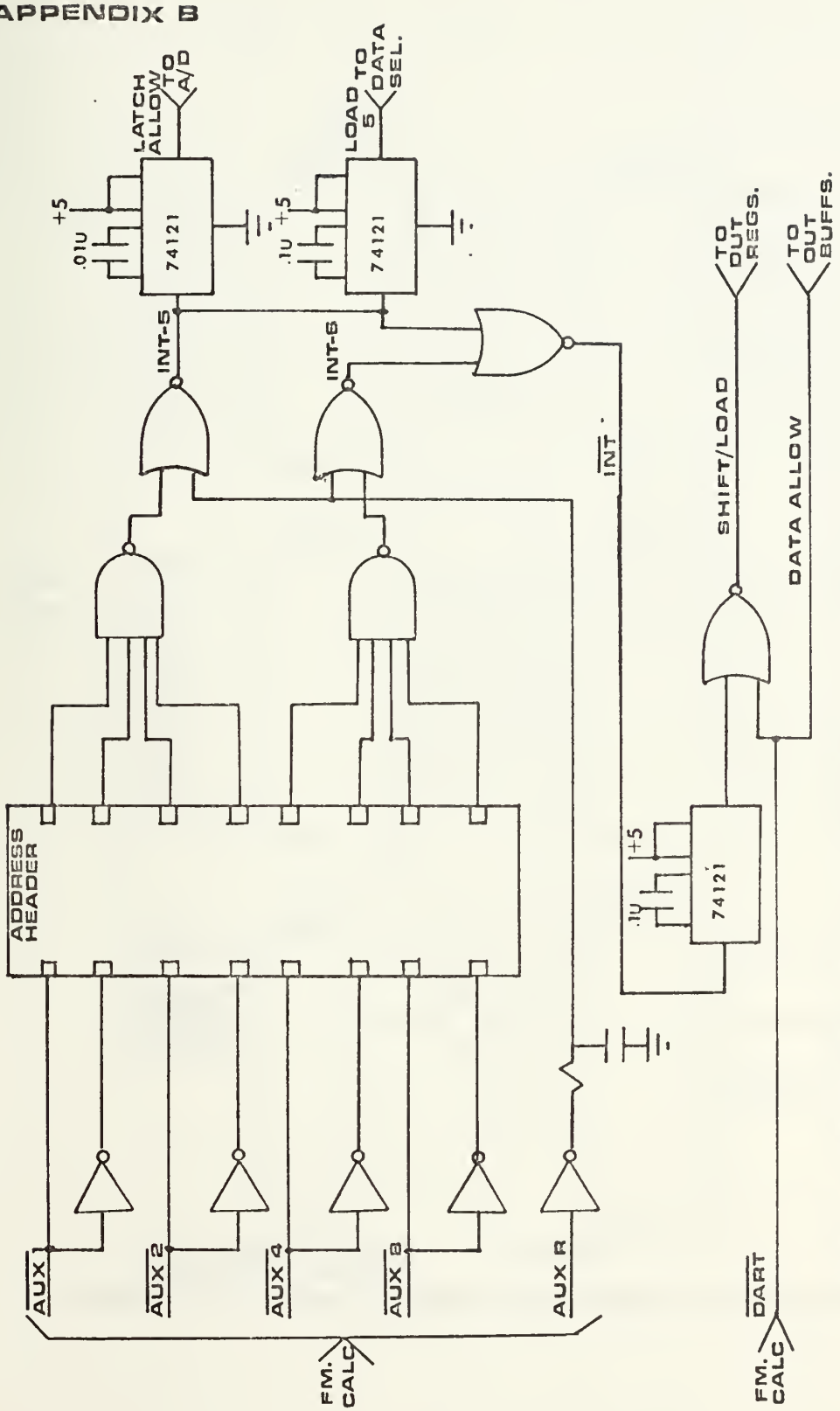


FIG.15 DECODER AND INTERFACE CONTROL

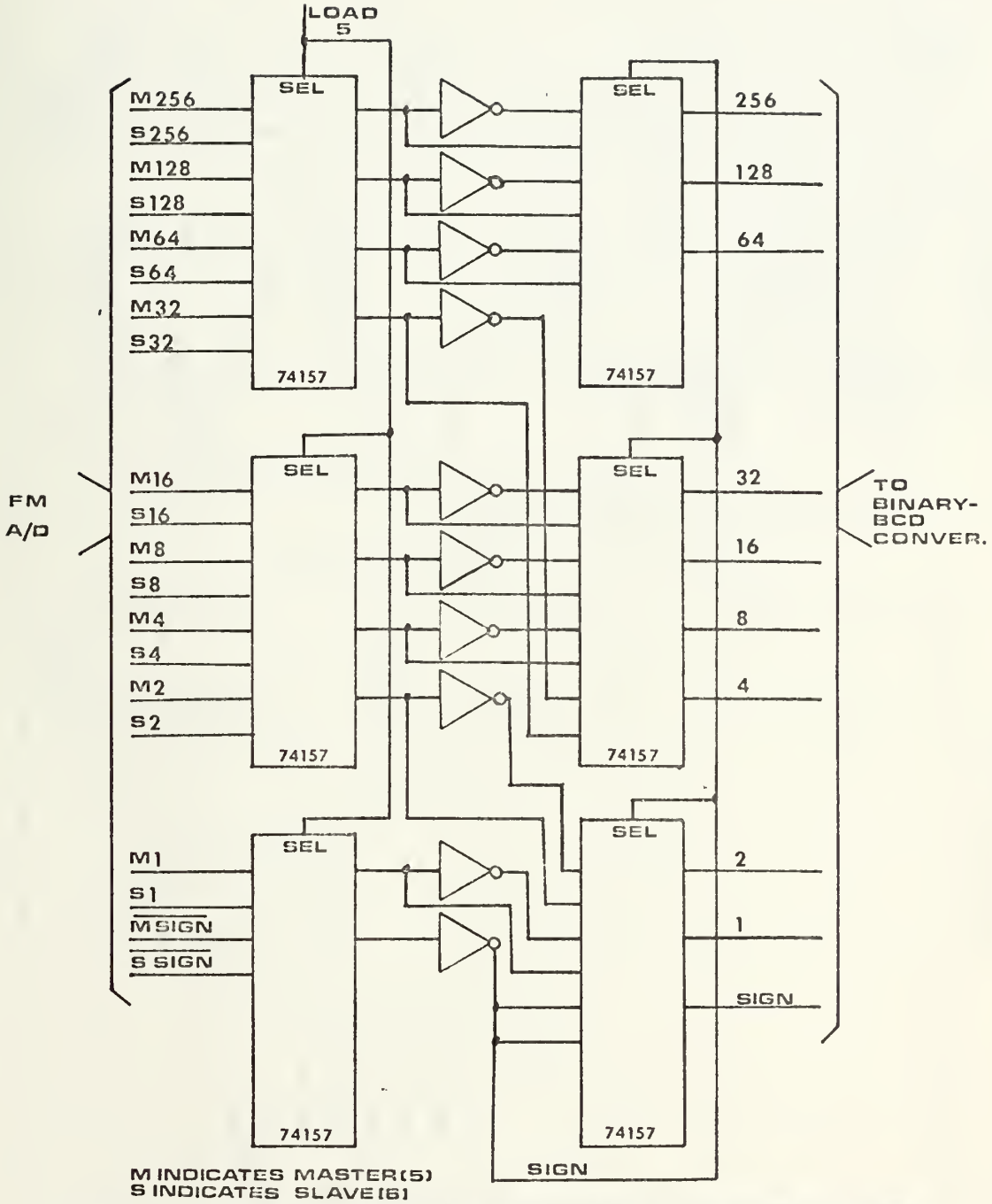


FIG.16 DATA SELECTOR AND SIGN CORRECTOR

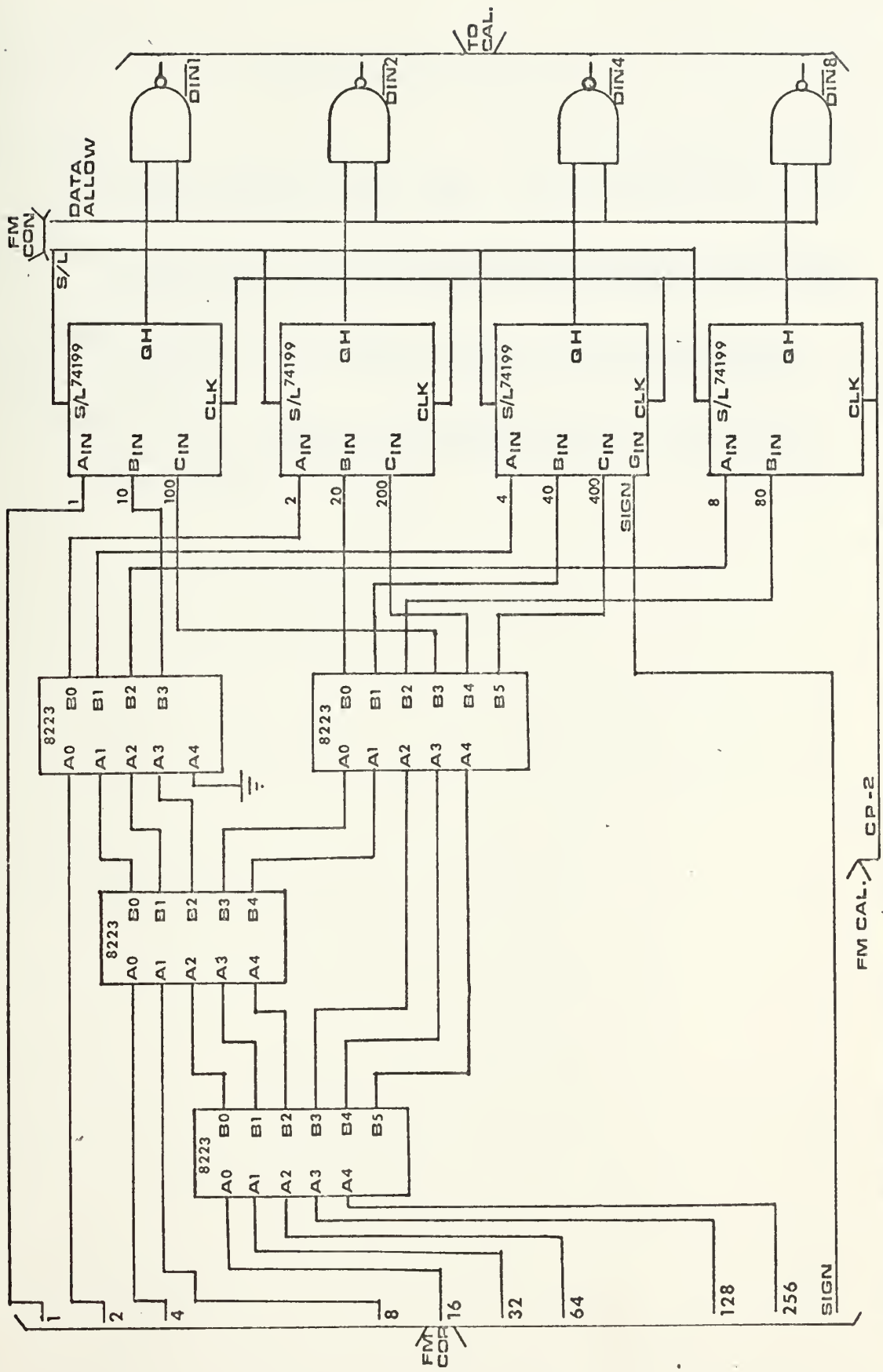


FIG.17 BINARY-BCD CONVERTER; OUTPUT REGS. AND BUFFS.

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13. ABSTRACT

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An investigation into the feasibility of using the 909, the A/D, and a D/A in the simulation of sampled data systems, or as a digital controller for a continuous plant was conducted.

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ata Processing						

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